## REMARKS

The Office Action mailed September 13, 2001, has been received and reviewed.

Claims 1-11, 13, 14, 16-35, 38, 40-41, 43, 44, 46-48, 51-61, 63, 66-82, 85, 87-88, and 91-98 are all the claims presently pending in the application, of which claims 91-98 have been withdrawn from consideration as being drawn to a non-elected invention. Claims 12, 14, 15, 36, 37, 39, 42, 45, 49, 50, 62, 64, 65, 83, 84, 86, 89, and 90 have been canceled.

Claims 1-11, 13, 14, 16-35, 38, 40-41, 43, 44, 46-48, 51-61, 63, 66-82, 85, 87-88, and 91-98 stand rejected, of which claims 1, 26, 51 and 76 are independent. Applicant has amended claims 1-3, 5, 7, 9, 11, 13, 16-19, 24-28, 30, 32, 34, 35, 38, 40, 41, 43, 51-53, 57, 59, 61, 63, 66-69, 74-76, 78, 81, 85, 87 and 88, and respectfully requests reconsideration of the application as amended herein.

### 35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Japanese Patent No. 6-151492

Claims 1 through 11, 16, 17, 26 through 36, 41, 42, 51 through 61, 66, 67, 76 through 82, and 88 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. 6-151492 assigned to Sony Corporation (hereinafter the "Sony reference"). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Sony reference discloses a first and second mold 1 and 2 opposing each other which forms a cavity 13 therebetween. A lead frame 5 with a semiconductor chip 15 mounted thereon is held in the cavity 13 which is oriented vertically. A resin 16 is then injected in the cavity at an underside thereof so that the resin 12 fills the cavity from the bottom to the top thereof. *See* Sony reference, Abstract and FIGS. 7-10.

However, the Sony reference does not teach (nor suggest) "positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of

said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate; and introducing a flowable material onto said at least one surface of said at least one semiconductor substrate in a substantially vertical direction in said at least one mold cavity so that said flowable material flows around said portions of said inner surface of said transfer mold abutting with said conductive elements on said at least one surface of said at least one semiconductor substrate," as recited in amended independent claim 1 (emphasis added). Rather, the Sony reference teaches a semiconductor chip 15 mounted to a lead frame 5 suspended in the transfer molds 1, 2 without such transfer molds 1, 2 abutting with the semiconductor chip. *See* Sony reference, Abstract, FIGS. 7-10. Thus, since amended independent claim 1 requires portions of the inner surface of the transfer mold to abut with the semiconductor substrate, amended independent claim 1 is not anticipated by the Sony reference. Applicant's therefore respectfully request the Examiner withdraw the rejection of independent claim 1.

In addition, independent claim 51 also has been amended with similar claim recitations to those of independent claim 1. Thus, Applicant respectfully submits that claim 51 should be patentable over the Sony reference for at least the same reasons as claim 1. With respect to dependent claims 2-11, 16, 17, 52-61, 66, and 67, they are patentable based on at least their respective dependencies from independent claims 1 and 51.

With respect to independent claim 26, the Sony reference does not teach (or suggest) "providing an assembly including at least one semiconductor device attached face down to a carrier substrate with conductive structures providing an assembly gap therebetween; [and] positioning said assembly in said at least one mold cavity of said transfer mold so that said carrier substrate abuts with a first inner surface of said transfer mold to provide an outer gap between a back surface of said at least one semiconductor device and an opposing second inner surface of said transfer mold; and introducing a flowable material onto at least one surface of said assembly to flow through said assembly gap and said outer gap in an upward, substantially vertical direction in said at least one mold cavity" Rather, the Sony reference teaches a lead frame assembly with the chip's back surface attached thereto without a gap between the chip and the lead frame. Further, Sony does not teach a flowable material flowing through the required gap. Thus, since independent claim 26 requires at least one semiconductor device attached face

down to a carrier substrate with an assembly gap therebetween and, a flowable material to flow through said assembly gap, independent claim 26 cannot be anticipated by the Sony reference. Applicant therefore respectfully requests the Examiner withdraw the rejection of independent claim 26.

In addition, independent claim 76 has been amended to recite similar recitations as that of independent claim 26. Therefore, claim 76 should be patentable over the Sony reference for at least the same reasons as independent claim 26. With respect to dependent claims 27-35, 41, 77-82, and 88, they are patentable based on at least their respective dependencies from independent claims 26 and 76. As to the rejection of dependent claims 36 and 42, such rejection is moot as claims 36 and 42 have been canceled.

**35 U.S.C. § 103(a) Obviousness Rejections**

Obviousness Rejection Based on Japanese Patent No. 6-151492 in View of U.S. Patent No. 5,471,369 to Honda et al.

Claims 12-15, 18-20, 22, 23, 37-40, 43-45, 47, 48, 62-65, 68-70, 72, 73, and 83-87 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent No. 6-151492 (hereinafter the "Sony reference") in view of Honda et al. (U.S. Patent No. 5,471,369). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 12-15, 18-20, 22, 23, 37-40, 43-45, 47, 48, 62-65, 68-70, 72, 73, and 83-87 should be removed because such claims depend from one of amended independent claims 1, 26, 51 and 76, each of which have been amended to include patentable recitations which are neither taught nor suggested by the Sony reference and

the Honda reference, alone and in combination, for reasons discussed below. As to the obviousness rejections of claims 12, 14, 15, 37, 39, 45, 62, 64, 65, 83, 84 and 86, such rejections are moot as these claims have been canceled.

As discussed previously, the Sony reference discloses a first and second mold 1 and 2 opposing each other which forms a cavity 13 therebetween. A lead frame 5 with a semiconductor chip 15 mounted thereon is held in the cavity 13 which is oriented vertically. A resin 16 is then injected in the cavity at an underside thereof so that the resin 12 fills the cavity from the bottom to the top thereof. *See* Sony reference, Abstract and FIGS. 7-10.

The Honda reference discloses multiple chips 43 attached to a die stage 44 or carrier substrate, wherein the chips 43 are electrically interconnected to a lead frame 48 partially extending in an encapsulant 42. The encapsulant 42 is formed through a transfer molding process in an arrangement where the chips 43 and die stage 44 are suspended in the encapsulant 42. *See* Honda, col. 7, lines 18-35; FIG. 8.

Turning first to independent claim 1, it has been amended to require that the semiconductor substrate is positioned in the transfer mold such that portions of the transfer mold abut the conductive elements on the at least one surface of the semiconductor substrate and a portion of the transfer mold abuts the back surface of the semiconductor substrate. Neither the Sony reference nor the Honda reference teach or suggest that which is recited in amended claim 1. Specifically, both the Sony reference and the Honda reference teach semiconductor chips attached to a lead frame, wherein such chips are positioned away from the inner surface of the transfer mold so that such chips are suspended therefrom to have the encapsulation formed around the outside surfaces of the chips. Therefore, the Sony reference and the Honda reference are deficient in the teaching or suggestion, alone and in combination, of each and every claim limitation of amended independent claim 1.

Furthermore, with respect to such deficiencies, there is no suggestion in the Sony reference and the Honda reference that would motivate a person of ordinary skill in the art to modify the positioning of the lead frame assembly in the transfer mold as taught in the references to overcome such deficiencies.

Thus, independent claim 1 is patentably distinguishable over the combination of the Sony reference and the Honda reference. In addition, independent claim 51 has been amended with similar claim recitations to those of claim 1 and, therefore, claim 51 should be patentably

distinguishable over the Sony reference and the Honda reference for the same reasons as independent claim 1. With respect to dependent claims 12-15, 18-20, 22, 23, 62-65, 68-70, 72 and 73, they are patentable over the Sony reference and the Honda reference based on at least their respective dependencies from claims 1 and 51.

With respect to independent claim 26, it has been amended to require an assembly with at least one semiconductor device attached face down to a carrier substrate with an assembly gap therebetween and further, claim 26 has been amended to require that the assembly is encapsulated in a transfer mold so that the assembly is positioned with the carrier substrate abutting a first inner surface of the mold and positioned with an outer gap between an opposing second inner surface of the mold and the back surface of the semiconductor device. In contrast, the Sony reference and the Honda reference, alone and in combination, neither teach nor suggest the limitations in claim 26 as amended. In particular, the Sony reference and the Honda reference teach lead frame assemblies in a transfer molding process, wherein each lead frame assembly is suspended away from the inner surface of the transfer mold during such transfer molding process. Thus, neither the Sony reference nor the Honda reference teaches or suggests the assembly in the positioned arrangement in a method of molding a semiconductor assembly, as recited in claim 26. Further, there is nothing taught or suggested in the Sony reference and the Honda reference that would motivate a person of ordinary skill in the art to modify the method of molding the assembly as disclosed in such references to the method recited in independent claim 26.

Thus, independent claim 26 is patentably distinguishable over the combination of the Sony reference and the Honda reference. In addition, independent claim 76 has been amended with similar claim recitations as that of claim 26 and, therefore, claim 76 should be patentably distinguishable over the Sony reference and the Honda reference for the same reasons as independent claim 26. With respect to dependent claims 37-40, 43-45, 47, 48 and 83-87, they are patentable over the Sony reference and the Honda reference based on at least their respective dependencies from claims 26 and 76.

Based on the foregoing reasons, the obviousness rejections of dependent claims 12-15, 18-20, 22, 23, 62-65, 68-70, 72 and 73 based on the Sony reference and the Honda reference should be removed since each of dependent claims 12-15, 18-20, 22, 23, 62-65, 68-70, 72 and 73 are patentable based on at least their dependency from independent claims 1, 26, 51 and 76.

Obviousness Rejection Based on Japanese Patent No. 6-151492 in View of U.S. Patent No. 6,081,997 to Chia et al.

Claims 21, 24, 25, 46, 49, 50, 71, 74, 75, 89, and 90 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent No. 6-151492 (hereinafter the "Sony reference") in view of Chia et al. (U.S. Patent No. 6,081,997). Applicant respectfully traverses this rejection, as hereinafter set forth.

Such rejection of claims 21, 24, 25, 46, 49, 50, 71, 74, 75, 89, and 90 should be removed because such claims depend from one of amended independent claims 1, 26, 51 and 76, each of which have been amended to include patentable recitations which are neither taught nor suggested by the Sony reference and the Chia reference, alone and in combination, for reasons discussed below. As to the obviousness rejections of claims 50, 89 and 90, such rejections are moot as these claims have been canceled. Independent claims 1, 26, 51 and 76 have been amended to be patentably distinguishable over the Sony reference and the Chi reference, alone and in combination.

As previously stated, the Sony reference discloses a first and second mold 1 and 2 opposing each which forms a cavity 13 therebetween. A lead frame 5 with a semiconductor chip 15 mounted thereon is held in the cavity 13 which is oriented vertically. A resin 16 is then injected in the cavity at an underside thereof so that the resin 12 fills the cavity from the bottom to the top thereof. *See* Sony reference, Abstract and FIGS. 7-10.

The Chia reference discloses a semiconductor assembly including a chip 12 mounted face down to a substrate 14 in a flip-chip type arrangement. The substrate 14 includes an opening 18 extending therethrough in a center location of the substrate 14. The assembly is placed in a mold having a first mold section 20 and a second mold section 26, wherein the first mold section 10 includes a mold opening 22 which is made to correspond with the opening 18 in the substrate 14. The assembly is therefore placed on the first mold section 20 with the opening 18 in the substrate 14 corresponding with the mold opening 22 of the first mold section 26. The second mold section is then placed over and against the back face of the chip 12. An encapsulant 32 is provided by pressurized injection through the openings 22 and 18 and then in the gap between the chip 12 and substrate 14 and to the periphery of the assembly. *See* Chia, col. 5, line 30 - col. 6, line 52; FIGS. 1-3.

Turning to independent claim 1, neither the Sony reference nor the Chia reference teach or suggest "positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate; . . . (emphasis added)" As previously discussed, the Sony reference discloses the inner surface of the mold as being separate from the chip since the Sony reference discloses a lead frame type assembly. The Chia reference teaches the second mold section 26 as abutting with the back surface of the chip 12, but the first mold section 20 is not positioned with "portions" abutting the conductive elements of the chip. Rather, the Chia reference discloses the first mold section abutting with the substrate 14.

Thus, the Sony reference and the Chia reference, alone and in combination, does not teach or suggest each and every limitation of claim 1, namely, the deficiency of "portions" of the inner surface of a mold abutting conductive elements on a semiconductor substrate. Further, since there is no teaching or suggestion in the Sony reference and the Chia reference of such deficiency, a person of ordinary skill in the art would not have been motivated to modify the methods disclosed in the references to overcome the deficiency.

In addition, independent claim 51 has been amended to recite similar claim recitations to those of claim 1 and, therefore, claim 51 should be patentably distinguishable over the Sony reference and the Chia reference for the same reasons as independent claim 1. With respect to dependent claims 21, 24, 25, 71, 74 and 75, they are patentable over the Sony reference and the Chia reference based on at least their respective dependencies from claims 1 and 51.

With respect to independent claim 26, it has been amended to require an assembly with at least one semiconductor device attached face down to a carrier substrate with an assembly gap therebetween, wherein the assembly is encapsulated in a transfer mold so that the assembly is positioned with the carrier substrate abutting a first inner surface of the mold and positioned with an outer gap between an opposing second inner surface of the mold and the back surface of the semiconductor device. Claim 26 further requires that the flowable material be introduced "through said assembly gap and said upper gap in an upward, substantially vertical direction in said at least one mold cavity."

In contradistinction to independent claim 26, the Chia reference does not include a gap between the outer surface of the chip 12 and the second mold section 26, and further, a flowable material that fills both "an outer gap" and "an assembly gap" in an "upward, substantially vertical direction." In addition, the Sony reference does not include an assembly as recited in independent claim 26, and therefore, the assembly disclosed in the Sony reference could not be positioned in the transfer mold as required by the method recited in claim 26. Thus, the Sony reference and the Chia reference, alone and in combination, does not teach or suggest each and every limitation as recited in claim 26. Furthermore, such deficient claim limitations in the proposed combination would not have been an obvious modification to a person of ordinary skill in the art since there is no suggestion of such deficiencies in either the Sony reference or the Chia reference.

In addition, independent claim 76 has been amended to recite similar claim recitations as that of claim 26 and, therefore, claim 76 should be patentably distinguishable over the Sony reference and the Chia reference for the same reasons as independent claim 26. With respect to dependent claims 46, 49, 50, 89, and 90 they are patentable over the Sony reference and the Chia reference based on at least their respective dependencies from claims 26 and 76.

Based on the foregoing reasons, the obviousness rejections of dependent claims 21, 24, 25, 46, 49, 50, 71, 74, 75, 89, and 90 based on the Sony reference and the Chia reference should be removed since each of dependent claims 12-15, 18-20, 22, 23, 62-65, 68-70, 72 and 73 should be patentable based on at least their dependency from independent claims 1, 26, 51 and 76.

Furthermore, amended dependent claims 24, 25, 74 and 75 are patentable over the Sony reference and the Chia reference in light of further limitations recited therein. Turning first to claims 24 and 74, the Sony reference and the Chia reference do not teach or suggest "portions of said inner surface of said transfer mold to comprise protrusions to abut with said conductive element on said at least one surface of said at least one semiconductor substrate," as recited in claims 24 and 74. Rather, the inner surface in the mold of the Sony reference is separated from the semiconductor chip by a gap of encapsulation material. The Chia reference discloses that the portion of the transfer mold in contact with the semiconductor chip is a flat surface and further, the transfer mold does not contact any of the conductive elements on the semiconductor chip. Thus, claims 24 and 74 are patentably distinguishable over the Sony reference and the Chia reference, alone and in combination, in light of further limitations recited therein.

With respect to claims 25 and 75, the Sony reference and the Chia reference do not teach or suggest "wherein said providing said at least one substrate comprises providing said at least one substrate having said at least one surface with conductive structures protruding therefrom, and wherein said providing said transfer mold comprises configuring each portion of said portions of said inner surface of said transfer mold to comprise a recess to at least partially receive a corresponding one of said conductive structures so that said flowable material partially covers said conductive structures," as recited in claims 25 and 75. Rather, the Chia reference discloses that the portion of the transfer mold in contact with the semiconductor chip is a flat surface (not a recess) and further, the transfer mold does not contact any of the conductive structures protruding from the semiconductor chip. As before, the Sony reference discloses that the inner surface in the mold is separated from the semiconductor chip by a gap of encapsulation material. Thus, claims 25 and 75 are patentably distinguishable over the Sony reference and the Chia reference, alone and in combination, for further reasons recited therein.

**Drawings**

Applicant submits herewith corrected formal drawings, under cover of a separate Transmittal of Formal Drawings. Applicant respectfully requests approval of the corrected formal drawings.

## ENTRY OF AMENDMENTS

The amendments to claims 1-3, 5, 7, 9, 11, 13, 16-19, 24-28, 30, 32, 34, 35, 38, 40, 41, 43, 51-53, 57, 59, 61, 63, 66-69, 74-76, 78, 81, 85, 87 and 88 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

## CONCLUSION

Claims 1-11, 13, 14, 16-35, 38, 40-41, 43, 44, 46-48, 51-61, 63, 66-82, 85, and 87-88 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,

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Enclosure: Version With Markings to Show Changes Made

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) A method of molding a semiconductor assembly [in a mold cavity of a transfer mold] comprising:

providing a transfer mold having an inner surface defining at least one mold cavity;

providing at least one semiconductor substrate having at least one surface with conductive elements thereon and a back surface thereof; [in said mold cavity; and]

positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate; and

introducing a flowable material onto said at least one surface of said at least one semiconductor substrate in a substantially vertical direction in said at least one mold cavity so that said flowable material flows around said portions of said inner surface of said transfer mold abutting with said conductive elements on said at least one surface of said at least one semiconductor substrate.

2. (Twice Amended) The method according to claim 1, [further comprising:] wherein said providing said transfer mold comprises configuring said transfer mold so that said at least one cavity is substantially vertically oriented with at least one gate at a lower portion of the transfer mold and at least one vent at an upper portion of the transfer mold [positioning said at least one substrate in at least one cavity of said transfer mold, said transfer mold having said at least one cavity substantially vertically oriented, said transfer mold including at least one gate at a lower portion of said at least one cavity and at least one vent at an upper portion thereof].

3. (Amended) The method according to claim 2, wherein said introducing said flowable material comprises:

substantially filling said at least one cavity in said substantially vertical direction.

5. (Amended) The method according to claim 2, wherein said positioning said at least one substrate further comprises:
positioning said at least one semiconductor substrate substantially vertically.

7. (Amended) The method according to claim 6, wherein said filling said at least one cavity with said flowable material comprises:
at least partially encapsulating said at least one semiconductor substrate.

9. (Amended) The method according to claim 1, wherein said introducing said flowable material comprises introducing said flowable material onto a substantially vertically oriented surface of said at least one semiconductor substrate.

11. (Amended) The method according to claim 1, wherein said providing said at least one substrate comprises:
providing an assembly including said at least one semiconductor substrate.

13. (Twice Amended) The method according to claim 11, wherein said providing said assembly comprises:
providing said assembly with said at least one semiconductor substrate comprising at least one semiconductor die having bond pads thereon, said at least one semiconductor die [being connected to a carrier] including [one of a carrier substrate and an interposer] conductive structures protruding from said bond pads.

16. (Amended) The method according to claim 1, wherein said providing said at least one semiconductor substrate comprises:
providing at least one individual semiconductor die.

17. (Twice Amended) The method according to claim 16, wherein said providing said at least one individual semiconductor die comprises:
providing said at least one individual semiconductor die with conductive structures protruding therefrom to abut with said portions of said at least one cavity.

18. (Twice Amended) The method according to claim [17] 1, wherein said providing said at least one [individual] semiconductor [die] substrate comprises:
providing a large-scale semiconductor substrate [including a plurality of semiconductor devices].

19. (Twice Amended) The method according to claim 18, wherein said providing said large-scale semiconductor substrate comprises:
providing [said large-scale substrate with said conductive structures protruding from bond pads of said plurality of semiconductor devices] a plurality of semiconductor dice interconnected to each other, each of said plurality comprising at least one of bond pads and conductive structures protruding from said bond pads.

24. (Amended) The method according to claim [2] 1, wherein [at least a portion] said providing said transfer mold comprises configuring said portions of said inner surface of said transfer mold to comprise protrusions to abut with said conductive element on said at least one surface of said at least one semiconductor substrate so that [of said at least one cavity prevents] said flowable material [from covering bond pads of] partially covers said at least one surface of said at least one semiconductor substrate.

25. (Amended) The method according to claim [2] 1, wherein said providing said at least one semiconductor substrate comprises providing said at least one semiconductor substrate having said at least one surface with conductive structures protruding therefrom, and wherein said providing said transfer mold comprises configuring each portion of said portions of said inner surface of said transfer mold to comprise a recess to [wherein said at least one cavity includes a cavity] at least partially [receiving] receive a corresponding one of said conductive structures [protruding from said at least one substrate and at least partially prevents] so that said flowable material [from covering] partially covers said conductive structures.

26. (Amended) A method of molding a semiconductor assembly [in a mold cavity of a transfer mold] comprising:
providing a transfer mold having an inner surface defining at least one mold cavity;

providing an assembly including at least one semiconductor device attached face down to a carrier substrate with conductive structures providing an assembly gap therebetween [at least one substrate having at least one surface in said mold cavity; and]

positioning said assembly in said at least one mold cavity of said transfer mold so that said carrier substrate abuts with a first inner surface of said transfer mold to provide an outer gap between a back surface of said at least one semiconductor device and an opposing second inner surface of said transfer mold; and

introducing a flowable material onto at least one surface of said assembly [at least one substrate] to flow through said assembly gap and said outer gap in an upward, substantially vertical direction in said at least one mold cavity.

27. (Twice Amended) The method according to claim 26, [further comprising:] wherein said providing said transfer mold comprises configuring said transfer mold so that said at least one cavity is substantially vertically oriented with at least one gate at a lower portion of the transfer mold and at least one vent at an upper portion of the transfer mold [positioning said at least one substrate in at least one cavity of said transfer mold, said transfer mold being configured with said at least one cavity substantially vertically oriented, said transfer mold including at least one gate at a lower portion of said at least one cavity and at least one vent at an upper portion thereof].

28. (Amended) The method according to claim 27, wherein said introducing said flowable material comprises:

substantially filling said at least one cavity in said upward, substantially vertical direction.

30. (Amended) The method according to claim 27, wherein said positioning said assembly [at least one substrate] further comprises:

positioning said assembly [at least one substrate] substantially vertically.

32. (Amended) The method according to claim 31, wherein said filling said at least one cavity with said flowable material comprises:

encapsulating said assembly [at least one substrate] so that said flowable material fills said assembly gap and said outer gap.

34. (Twice Amended) The method according to claim 26, wherein said introducing said flowable material comprises said flowable material to flow substantially across said at least one surface of said assembly [at least one substrate].

35. (Twice Amended) The method according to claim 26, wherein said introducing said flowable material onto said at least one surface of said assembly [at least one substrate] in said upward, substantially vertical direction comprises substantially preventing voids in said flowable material.

38. (Twice Amended) The method according to claim 26 [36], wherein said providing said assembly comprises:

providing said assembly with said [at least one substrate including at least one semiconductor die, said] at least one semiconductor device [die being] connected to [a carrier including one of a carrier substrate and] an interposer.

40. (Twice Amended) The method according to claim 26 [39], wherein said introducing said flowable material comprises:

introducing said flowable material to flow between said at least one semiconductor device [die] and said carrier substrate.

41. (Amended) The method according to claim 26, wherein said providing said assembly [at least one substrate] comprises:

providing at least one individual semiconductor die.

43. (Twice Amended) The method according to claim 26 [42], wherein said providing said assembly [at least one individual semiconductor die] comprises:

providing a large-scale substrate including a plurality of semiconductor devices attached face down thereto.

51. (Twice Amended) A method for encapsulating a substrate that substantially prevents voids in an encapsulant, [in a transfer mold having at least one cavity,] the method comprising:

providing a transfer mold having an inner surface defining at least one mold cavity;

providing at least one semiconductor substrate having at least one surface with conductive elements thereon and a back surface thereof; [and]

positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate; and

introducing a flowable material onto at least one surface of said at least one substrate in an upward, non-horizontal direction in said at least one mold cavity so that said flowable material flows around said portions of said inner surface of said transfer mold abutting with said conductive elements on said at least one surface of said at least one substrate.

52. (Amended) The method according to claim 51, [further comprising:

positioning said at least one substrate in said at least one cavity of said transfer mold, said transfer mold having said at least one cavity non-horizontally oriented and including at least one gate at a lower portion of said at least one cavity and at least one vent at an upper portion thereof] wherein said providing said transfer mold comprises configuring said transfer mold so that said at least one cavity is non-horizontally oriented with at least one gate at a lower portion of the transfer mold and at least one vent at an upper portion of the transfer mold.

53. (Amended) The method according to claim 52, wherein said introducing said flowable material comprises:

substantially filling said at least one cavity in a non-horizontal direction.

57. (Amended) The method according to claim 56, wherein said filling said at least one cavity with said flowable material comprises:

at least partially encapsulating said at least one substrate.

59. (Twice Amended) The method according to claim 51, wherein said introducing said flowable material comprises permitting said flowable material to flow onto a substantially vertically oriented surface of said at least one semiconductor substrate.

61. (Amended) The method according to claim 51, wherein said providing said at least one substrate comprises:
providing an assembly including said at least one semiconductor substrate.

63. (Twice Amended) The method according to claim 61, wherein said providing said assembly comprises:
providing said assembly with said at least one semiconductor substrate including at least one semiconductor die having bond pads thereon, said at least one semiconductor die [being connected to a carrier including one of a carrier substrate and an interposer] including conductive structures protruding from said bond pads.

66. (Amended) The method according to claim 51, wherein said providing said at least one semiconductor substrate comprises:
providing at least one individual semiconductor die.

67. (Twice Amended) The method according to claim 66, wherein said providing said at least one individual semiconductor die comprises:
providing said at least one individual semiconductor die with conductive structures protruding therefrom to abut with said portions of said at least one cavity.

68. (Twice Amended) The method according to claim [67] 51, wherein said providing said at least one [individual] semiconductor [die] substrate comprises:
providing a large-scale semiconductor substrate [including a plurality of semiconductor devices].

69. (Twice Amended) The method according to claim 68, wherein said providing said large-scale semiconductor substrate comprises:

providing [said large-scale substrate with said conductive structures protruding from bond pads of said plurality of semiconductor devices] a plurality of semiconductor dice interconnected to each other, each of said plurality comprising at least one of bond pads and conductive structures protruding from said bond pads.

74. (Amended) The method according to claim 51, [52, wherein said at least one cavity prevents] said providing said transfer mold comprises configuring said portions of said inner surface of said transfer mold to comprise protrusions to abut with said conductive element on said at least one surface of said at least one semiconductor substrate so that said flowable material [from covering bond pads of] partially covers said at least one surface of said at least one semiconductor substrate.

75. (Twice Amended) The method according to claim 51, [52, wherein a portion of said at least one cavity] wherein said providing said at least one semiconductor substrate comprises providing said at least one semiconductor substrate having said at least one surface with conductive structures protruding therefrom, and wherein said providing said transfer mold comprises configuring each portion of said portions of said inner surface of said transfer mold to comprise a recess to at least partially receive [receives] a corresponding one of said conductive structures [protruding from said at least one substrate and at least partially prevents] so that said flowable material partially covers [from covering] said conductive structures.

76. (Amended) A method for transfer molding a semiconductor assembly [at least one semiconductor device component, the method] comprising:

providing at least one transfer mold having an inner surface defining at least one cavity, said at least one transfer mold [cavity] including at least one gate at a lower portion thereof and at least one vent at an upper portion thereof;

providing an assembly including at least one semiconductor device attached face down to a carrier substrate with conductive structures providing an assembly gap therebetween;

positioning said assembly in said at least one mold cavity of said transfer mold so that said carrier substrate abuts with a first inner surface of said transfer mold to provide an outer

gap between a back surface of said at least one semiconductor device and an opposing second inner surface of said transfer mold; and

[positioning at least one substrate within said at least one cavity; and]

introducing a resin material into said at least one cavity through said at least one gate so that said resin material moves upwardly over said assembly and through said assembly gap and said outer gap [at least one substrate] in a non-horizontal direction.

78. (Twice Amended) The method according to claim 76, wherein said introducing said resin material comprises:

at least partially encapsulating said assembly [at least one substrate].

81. (Twice Amended) The method according to claim 76, wherein said introducing said resin material includes a single, substantially uniform flow front around said assembly [at least one substrate].

85. (Twice Amended) The method according to claim 76 [84], wherein said providing said assembly comprises:

providing [said assembly including] a flip-chip type semiconductor device.

87. (Twice Amended) The method according to claim [86] 76, wherein said introducing said resin material comprises:

introducing said resin material to flow between said semiconductor device and said carrier substrate.

88. (Twice Amended) The method according to claim 87, wherein said introducing said resin material further comprises:

at least partially encapsulating at least one of said semiconductor device and said carrier substrate.